

Transferrable, wet-chemistry-derived high-*k* amorphous metal oxide dielectrics for two-dimensional electronic devices

Received: 5 October 2024

Accepted: 30 January 2025

Published online: 10 February 2025

 Check for updates

Zhixin Yao^{1,2,8}, Huifeng Tian^{2,8}, U. Sasaki², Huacong Sun³, Jingyi Hu², Guodong Xue⁴, Ye Seul Jung⁵, Ruijie Li², Zhenjiang Li², PeiChi Liao², Yihan Wang², Lina Yang Zhang², Ge Yin², Xuanyu Zhang², Yijie Luo², Wenxi Li², Yong Soo Cho⁵, Peizhi Liu¹, Kaihui Liu^{4,6}, Yanfeng Zhang², Lifan Wang^{3,7}, Junjie Guo^{1,9}✉ & Lei Liu^{2,6,9}✉

Two-dimensional (2D) materials hold transformative potential for next-generation electronics. The integration of high dielectric constant (*k*) dielectrics onto 2D semiconductors, while maintaining their pristine properties by low-defect-density interfaces, has proven challenging and become one performance bottleneck of their practical implementation. Here, we report a wet-chemistry-based method to fabricate amorphous, transferable high-*k* (42.9) copper calcium titanate (CCTO) thin films as high-quality, dual-function dielectrics for 2D electronic devices. The chelation-based Pechini approach guarantees uniformity in this perovskite-type complex oxide, while the transferrable feature allows its harmless integration to 2D semiconductors interfacing with a nanogap. The CCTO-gated MoS₂ devices exhibit a sub-threshold swing down to 67 mV dec⁻¹ and an ultra-small hysteresis of ~1 mV/(MV cm⁻¹). Moreover, leveraging its visible-light active characteristics, we implement an electrically-manipulated, optically-activated nonvolatile floating gate in CCTO, enabling the reconfigurable execution of 9 basic Boolean logic in-sensor operations within a single field-effect device architecture. This advancement paves the way for the development of multifunctional, low-power 2D electronic systems by incorporating multifunctional conventional complex oxides.

Two-dimensional (2D) semiconductors, as exemplified by transition metal dichalcogenides (TMDs), have gradually delivered their potential to ease the significant challenges silicon integrated circuits encounter, that is, increasingly scaled size, heat, and memory walls^{1–3}. Performances

of both field-effect transistors (FETs) and memory devices can be boosted by leveraging 2D semiconductors' characteristics, mainly including the atomic-scale thickness allowing exceptional electrostatic control and the dangling-bond-free surface with van der Waals (vdW)

¹Key Laboratory of Interface Science and Engineering in Advanced Materials, Ministry of Education, Taiyuan University of Technology, Taiyuan, China. ²School of Materials Science and Engineering, Peking University, Beijing, China. ³Beijing National Laboratory for Condensed Matter Physics, Institute of Physics, Chinese Academy of Sciences, Beijing, China. ⁴State Key Laboratory for Mesoscopic Physics, Frontiers Science Centre for Nano-optoelectronics, School of Physics, Peking University, Beijing, China. ⁵Department of Materials Science and Engineering, Yonsei University, Seoul, Republic of Korea. ⁶Interdisciplinary Institute of Light-Element Quantum Materials and Research Center for Light-Element Advanced Materials, Peking University, Beijing, China. ⁷Songshan Lake Materials Laboratory, Dongguan, Guangdong, China. ⁸These authors contributed equally: Zhixin Yao, Huifeng Tian. ⁹These authors jointly supervised this work: Junjie Guo, Lei Liu. ✉e-mail: guojunjie@tyut.edu.cn; l.liu@pku.edu.cn

interactions responsible for the Lego-type integration⁴. Recently, all-in-one perceptual, memory and computational fusing in 2D devices have achieved tremendous success by creating technologies beyond von Neumann architecture, enabling in-sensor/memory computing for, e.g., image and acoustic pattern recognition and processing^{1,5,6}.

The vdW surface of 2D semiconductors, however, also leads to one critical challenge: integrating high-quality, high-*k* dielectrics as silicon did. For conventional amorphous high-*k* dielectrics, including hafnium oxide (HfO₂) and aluminum oxide (Al₂O₃), the absence of dangling bonds on 2D surfaces results in poor nucleation during the direct deposition methods such as atomic layer deposition (ALD), leading to suboptimal interface quality characterized by increased defects and undesirable doping to TMDs layers⁷. Thus, a buffer/seeding layer had to be performed first for ALD process^{8,9}. CaF₂ epitaxially grown also by the gas-to-solid method has been demonstrated as excellent dielectrics for the back-gate configuration¹⁰. On the other side, by using the transfer technique, one can feasibly separate the fabrication and integration of dielectrics, loosening restrictions in dielectric elements and synthesis temperatures but asking for its transferrable feature^{11–16}. For instance, single-crystal perovskite strontium titanium oxide (SrTiO₃), which holds a high static permittivity, can be first fabricated on sacrificial layers by pulsed laser deposition and then transferred as a freestanding flake to be incorporated into TMDs devices^{17,18}. More importantly, in these devices, the omnipresent nanogap between TMDs and transferred oxides denies physical contact with the channel materials and also suppresses the gate leakage currents, allowing metal oxides with moderate bandgaps (3.3 eV for SrTiO₃, and 3.8 eV for Sr₂Nb₃O₁₀) as good dielectrics that's somewhat counterintuitive^{17–19}.

In the context of all-in-one in-sensor computing in 2D devices, one will expect that one certain layer in heterostructures is a sensing layer, for example, sensitively responsible to external stimuli (such as optical, electrical, and thermal ones) and effectively transferring this signal to neighboring layers, or even a multifunctional layer to reduce the layer number and simply the structure²⁰. Deeply engineering the dielectric layer by rendering it multifunctional (beyond dielectric) is worth exploring²¹. When used as a component in 2D devices, the traditional dielectrics prepared by the gas-to-solid method are limited in material types and functions because of either the restricted gaseous precursors or the transferable prerequisite. On a parallel front, metal oxides obtained from the liquid-to-solid approach, i.e., the wet chemistry, are low-cost, massively prepared, and, more importantly, versatile in category and function, being widely used in thin-film electronics, including displays and sensors, and multi-energy areas like capacitors and batteries^{22,23}. Merging two broad trajectories in separate fields, solution-processed metal oxides as dielectrics in 2D devices, remains an unexplored regime, and it can in principle offer more possibilities and candidates for advanced 2D electronics if the resulting metal oxides are compatible with 2D technology, for example, being able to be transferred and vdW integrated to form heterostructures.

In this work, we report a wet-chemistry-derived method to unprecedentedly prepare amorphous copper calcium titanate (CCTO), a perovskite-type complex oxide, which can be transferred and further incorporated into 2D devices. Benefiting from its superior dielectric properties and the nanogap between transferred oxides and 2D semiconductors, CCTO/TMDs devices exhibit a subthreshold swing (SS) of 67 mV dec⁻¹ and ultra-small hysteresis (-1 mV/(MV cm⁻¹), corroborating a high-quality CCTO-2D materials interface. Furthermore, utilizing the optical properties of CCTO, in a simple FET device, optically writing and electrically erasing the floating gate are achieved, leading to a reconfigurable logic-in-sensor operation.

Results

Pechini-based synthesis

Compared with common simple oxide dielectrics (e.g., HfO₂) with *k* typically less than 30, some complex oxides can possess ultrahigh *k*,

for example, 100–300,000 for crystalline CCTO, as previously reported^{24,25}. CCTO has a double-perovskite structure, with both Ca²⁺ and Cu²⁺ located on the A site and Ti⁴⁺ placed on the B site (Supplementary Fig. 1a). One key challenge in fabricating these multi-metal oxides is the phase-separation-induced spatial inhomogeneity, which detrimentally affects the uniformity^{26,27}. To this end, the Pechini method, one widely utilized sol-gel route, was selected. As sketched in Fig. 1a, after mixing aqueous solutions of commonly used metal salts, each metal cation can be chelated by citric acid to form complex ring-shaped compounds around metal cations, therefore ensuring the intimate mixing on the atomic scale in solution. After adding ethylene glycol and spin coating the solution on substrates, a low-temperature baking treatment (typically -150 °C and 10 min) removes excess water, simultaneously allowing chelates to polymerize and form a cross-linked and large network. The resin decomposes by elevating the calcination temperature, and the organic components are removed, producing a large-scale thin film of amorphous oxides (Methods). In this way, the metal cations refrain from aggregating in precursors to obtain a good distribution of cations on the atomic level, eventually ensuring the compositional homogeneity in calcine thin films²⁸.

By simply tuning the concentration of inorganic precursors and/or rotational speed, the thickness of thin films can be well controlled in the range of 15–50 nm by a single run of the spin-coating process (Supplementary Fig. 1b, c). Films with a thickness of several hundred nm can also be prepared by repeating the spin coating process (Supplementary Fig. 1d). Moreover, the calcination temperature *T_c* was able to control the degree of crystallinity, and we thereby labeled the CCTO samples by *T_c*, for example, CCTO films calcinated at 300 °C as CCTO-300. By X-ray photoemission spectroscopy (XPS) measurements on CCTO films obtained at low temperatures (≤300 °C, Supplementary Fig. 2), we noticed that very likely 300 °C was the lowest temperature for a complete Pechini reaction. By Raman and X-ray diffraction (XRD) characterizations (Supplementary Fig. 3), we found that CCTO films calcinated below 600 °C were amorphous, while CCTO-600 had a spatially hybrid crystalline-amorphous structure and pure crystalline phase for CCTO films at 700 °C and above. Note that the temperature-dependent crystallinity of CCTO thin films observed here is consistent with that of CCTO powders reported previously²⁹.

Due to the solution process and spin-coating deposition, the as-obtained CCTO film has 100% coverage on substrates. Strikingly, when applying the transfer technique originally established for 2D materials, including the protection of polymer layers and wet etching of the underlying substrate, the whole CCTO thin film can be detached from the substrate, suspended on water, and then transferred onto a target substrate integrally (Fig. 1b, see details in “Methods”; Supplementary Fig. 4). While the Pechini method is a one well-established and industrially-used way to prepare various complex metal oxides, to the best of our knowledge previously no one has shown the preparation of transferable thin films of complex metal oxides by the Pechini method. This process bears a high level of resemblance to transferring a large-area, layered 2D material, offering the chance to incorporate this Pechini-derived oxide thin film into heterostructures with 2D materials. We first investigate the possible quality degradation of CCTO films induced by the transfer process (Supplementary Note 1 and Supplementary Figs. 5–7); results confirm the preservation of films' qualities after transfer. Moreover, good surface roughness is also a prerequisite for constructing heterostructures. As presented in Fig. 1c, atomic force microscope (AFM) measurements on a CCTO film show a flat, uniform surface free of wrinkles or other impurities with a root mean square (RMS) of 0.129 nm. We further list histograms of the height distributions over a large area (3 × 3 μm) for a bare SiO₂/Si substrate, a CCTO thin film (one layer, 1 L), and a thick film (five layers, 5 L by repeating the spin-coating process five times), respectively, with the Gaussian fits to the distributions³⁰. While thin film manifested itself with a slightly smaller roughness than that of SiO₂/Si substrates, the thicker film can

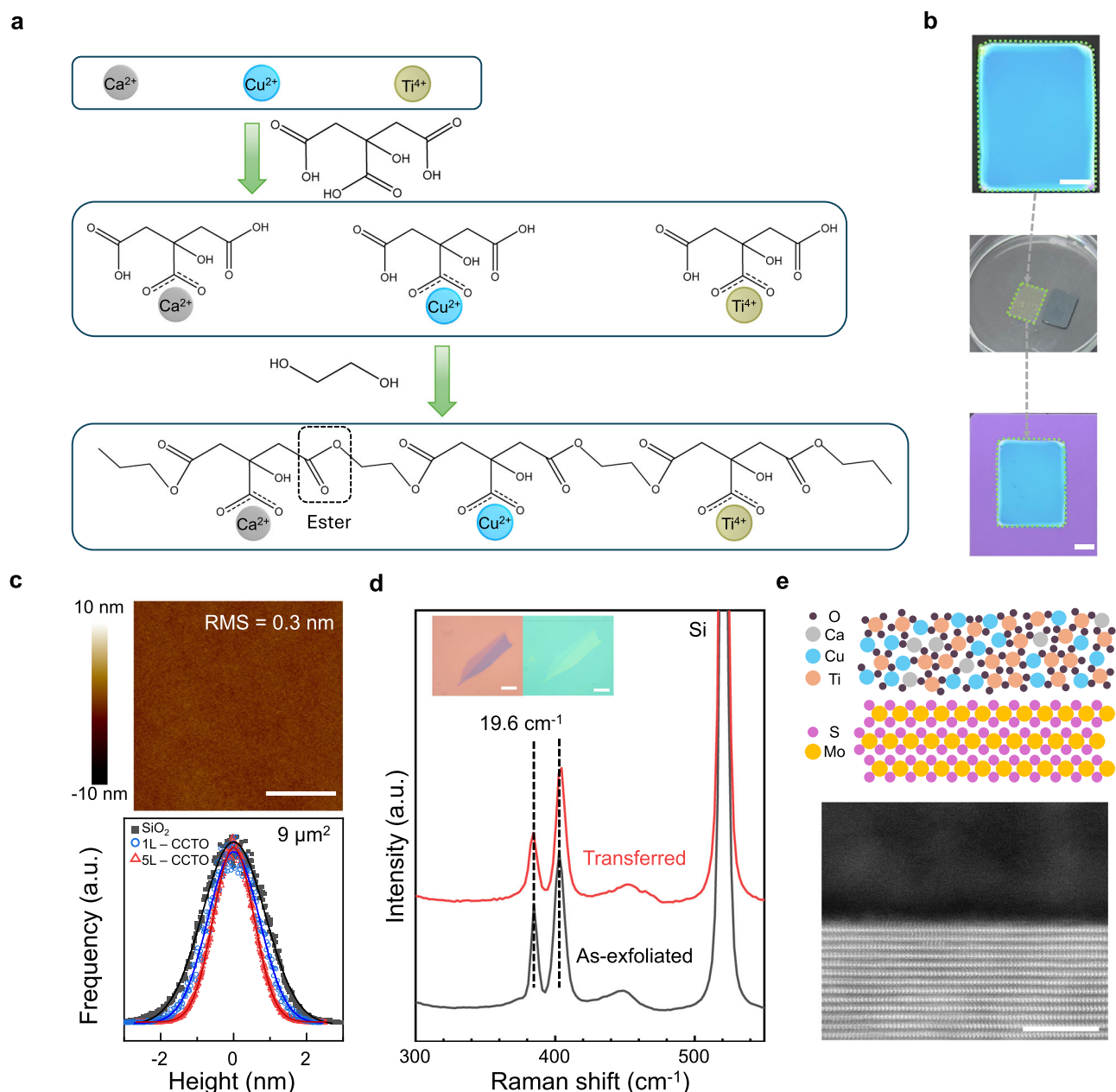


Fig. 1 | Preparation and transfer of Pechini-derived CCTO films. **a** Schematic of the Pechini process, mainly including the chelation of single metal cations by citric acid and the polymerization of the chelates initiated by ethylene glycol. **b** Representative optical images of as-prepared amorphous CCTO thin films on a SiO₂/Si wafer (top panel), the detachment of one PMMA-protected CCTO film from the original substrate (middle panel), and the transferred film on a target substrate (bottom panel). Scale bars: 3 mm. **c** Typical AFM image (top panel) and histograms

of the height distributions over a relatively large area (9 μm²) on surfaces of SiO₂, 1L-CCTO, and 5L-CCTO films, respectively. Solid lines are Gaussian fits to these distributions. Scale bars: 1 μm. **d** Raman spectra of one MoS₂ flake before and after transferring a CCTO film on top. Insets: optical images of the MoS₂ samples on a SiO₂/Si substrate (left) and covered by a transferred CCTO film (right). Scale bars: 10 μm (inset). **e** Schematic and STEM image of a CCTO/MoS₂ heterostructure. Scale bars: 5 nm.

be treated as freestanding and free of the clamping from substrate roughness, showing even smoother surfaces. While the energy minimization criterion demands a certain equilibrium polyhedral shape for a crystal, one well-known fact is that its amorphous counterpart naturally possesses a geometry of smooth surfaces without vertexes or facets, one macroscopic-scale discrepancy between crystallites and glassy materials³¹. We also note that the ramping rate of the calcination was typically programmed to be as low as 5 °C/min, which could also be responsible for its smooth surface.

The next thing we considered was the integration method (Supplementary Note 2 and Supplementary Fig. 8). By the transfer process one can easily form CCTO/MoS₂ stacks; as shown in Fig. 1d, the

difference in peak positions between A_1' (out-of-plane) and E' (in-plane) vibrational modes is 19.6 cm⁻¹ for the as-exfoliated MoS₂ flake (before transfer) and the same one in the CCTO/MoS₂ heterostructure (after transfer). This finding confirms the absence of apparent micron-scale structural damages in the exfoliated MoS₂ flake after the transfer integration^{32,33}. Furthermore, by using the combination of a focused ion beam (FIB) and scanning transmission electron microscope (STEM), the cross-sectional structures of CCTO/MoS₂ heterostructures were investigated. As displayed in Fig. 1e, there is no physical contact between the CCTO and MoS₂ flake. Further by the element mapping (Supplementary Fig. 9), a nanogap with a width of ~1 nm is confirmed, consistent with the nanogap observed between the transferred

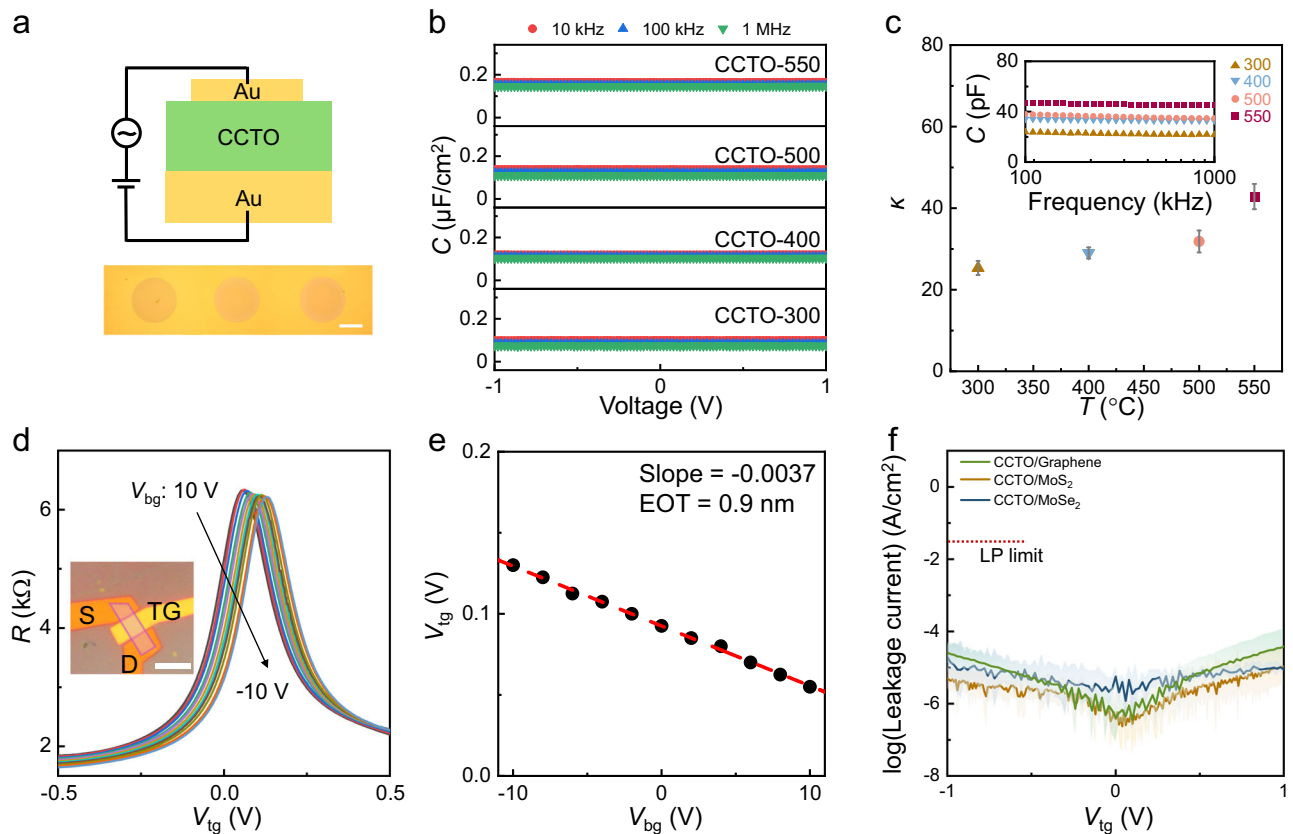


Fig. 2 | Dielectric properties of Pechini-derived CCTO thin films. **a** Schematic (top panel) and top-view optical image (bottom panel) of MIM devices for C - V measurements. Scale bars: 100 μm . **b** Capacitance versus voltage with different frequencies for various CCTO samples. **c** Calculated k at 100 kHz as a function of films' calcination temperatures. Inset: C versus frequency in the range of 100 kHz–1 MHz for various CCTO samples, showing flat curves to consider the distributed model for border traps. **d** Top-gate transfer characteristics of one monolayer graphene FET with a transferred CCTO-550 film (thickness: 8 nm) as top-

gate dielectrics. Inset: Optical image of the dual-gate monolayer graphene FET with a bottom-gate length of 6.62 μm and top-gate length of 5.73 μm . Scale bars: 10 μm (inset). **e** Top-gate Dirac point voltage as a function of V_{bg} . The red dotted line shows linear fitting of the experiment data. The slope is -0.0037 , corresponding to equivalent oxide thickness of 0.9 nm. **f** Statistics of top leakage currents from three types of dual-gated transistors with transferred, 15 nm thick CCTO-550 films as top-gate dielectrics.

dielectrics and TMDs flake^{17–19}. The origin of this nanogap could be ascribed to the adsorbed adlayers (e.g., oxygen and water), which have been utilized to precisely control the gap size up to 5–6 nm^{14,34}.

Dielectric properties

To quantitatively evaluate the dielectric properties of Pechini-derived CCTO thin films, we applied the measurements on CCTO films by metal-insulator-metal (MIM) parallel capacitors. CCTO films were first transferred onto Au substrates, followed by the deposition of top Au circle electrodes (Fig. 2a). For CCTO films obtained at 300–550 $^{\circ}\text{C}$, the capacitance C was measured versus the frequency and analyzed based on multiple MIM devices. For CCTO samples obtained at each calcination temperature, at least ten devices were selected from different preparation batches. As shown in Fig. 2b, the measured capacitance keeps constant within the applied voltage (-1 – 1 V). With the calcination temperature increased, the film's capacitance increased, which agrees well with results of CCTO pellets and is believed to be a consequence of the improved crystallinity³⁵. Furthermore, calculations of films' k were conducted based on the equation $C = S\epsilon_0 k/d$, where S is the area of the top electrode, ϵ_0 is the vacuum permittivity, and d is the thickness of the film (measured by AFM in our experiments), and are listed as the functions of calcination temperatures at 100 kHz in Fig. 2c. Results show that k of all CCTO thin films we investigated is higher than 20 with a small variation to exclude a significant point-to-point difference, and for CCTO-550 k reaches 42.9. This result, in accordance with its high dielectric performance reported previously, unambiguously

confirms the high- k nature of the Pechini-derived CCTO thin films. By further using the distributed model for border traps in which, at high frequencies, C becomes constant and insensitive to frequency with no border trap contributions (here, 100 kHz–1 MHz for CCTO-550 thin films, as shown in the inset of Fig. 2c)^{7,36}, k of CCTO-550 is 41.1 after deducting the contribution from border traps, demonstrating the pristine high- k nature of CCTO. Furthermore, the C - V characterizations were performed on CCTO films prepared on Au (no transfer required) and the SiO_2/Si substrate (then transferred onto Au substrates for C - V measurements), respectively, and no discrepancy in C - V curves was found between the two samples (Supplementary Fig. 10), highly suggesting the absence of dielectric property deteriorations induced by the transfer process. Furthermore, the electrical breakdown behaviors were also investigated (Supplementary Fig. 11).

The practicality of its high- k functionality was further examined for CCTO thin films as top-gate dielectrics in dual-gated monolayer graphene FETs. As exemplified by CCTO-550 thin films which were transferred on top of monolayer graphene (Fig. 2d), the channel resistance R exhibits the standard, ambipolar characteristic upon the top-gate voltage (V_{tg}) with its maximum (charge neutrality point) at the top-gate Dirac point voltage ($V_{\text{tg, D}}$), corroborating the dielectric functionality of CCTO thin films in 2D material devices. Since the charge carrier density in graphene can be modulated separately by top and bottom gates, by varying the bottom-gate voltage V_{bg} , the top-gate transfer characteristics shift accordingly and as well as $V_{\text{tg, D}}$. The relationship between the top gate Dirac point voltage and the back

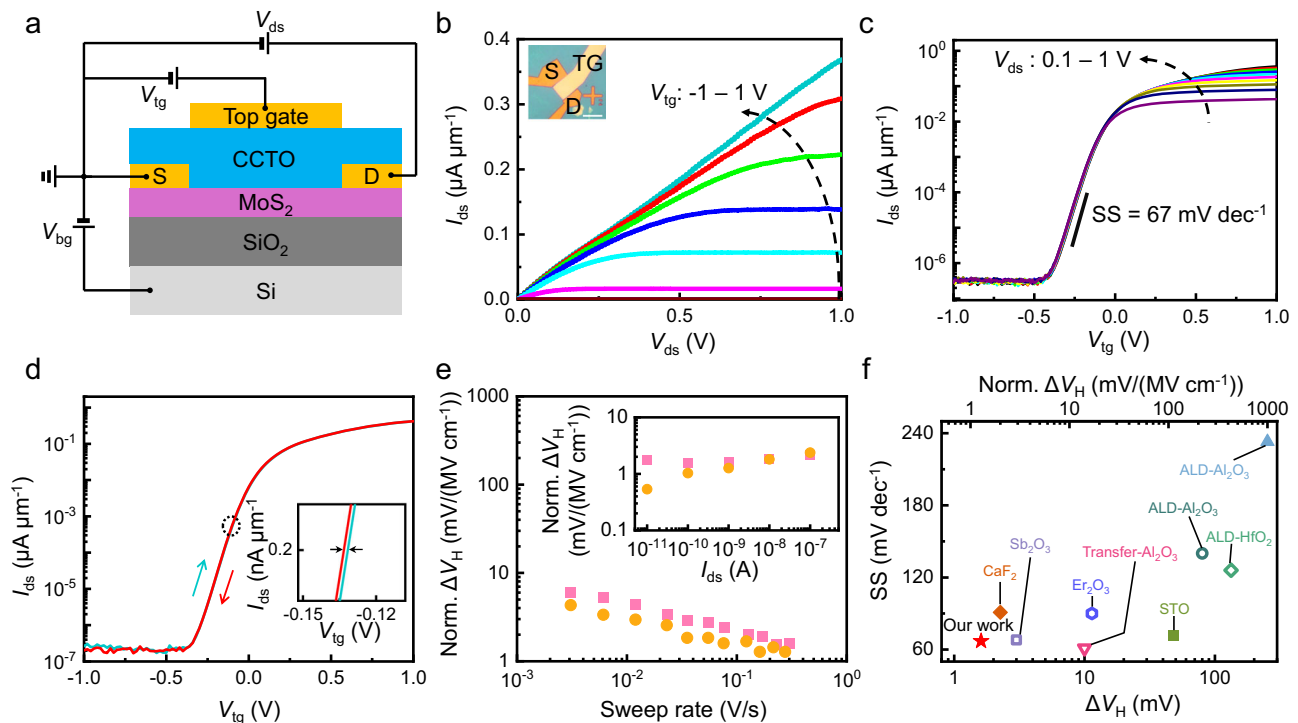


Fig. 3 | Device performance of CCTO-gated MoS₂ devices. **a** Schematic of the device configuration. **b** I_{ds} - V_{ds} characteristics measured for one exfoliated MoS₂ flake (thickness: 2.4 nm) top-gated by a transferred, 15 nm thick CCTO-550 thin film. Inset: optical image of one as-fabricated device. Scale bar: 10 μm (inset). **c** Transfer curves of the CCTO/MoS₂ device under various V_{ds} , showing an ultra-small SS of 67 mV dec⁻¹. **d** Double-sweep transfer curve under $V_{ds} = 1$ V, displaying a negligible

hysteresis. **e** Norm. hysteresis width ΔV_H versus the sweep rates under two different V_{tg} ranges (gold: $V_{tg} = -2$ V– 2 V, pink: $V_{tg} = -1$ V– 1 V). Inset: Norm. ΔV_H as a function of I_{ds} (sweep rate: 0.3 V/s). **f** A comparison of SS and Norm. ΔV_H of our CCTO-gated MoS₂ devices with other high- k dielectrics reported in the literature (Supplementary Table 3). Note that filled (open) symbols correspond to norm. ΔV_H (ΔV_H)^{10,13,18,39,40,42,45,46}.

gate voltage is shown in Fig. 2e, with a linear fit indicating a slope of -0.0037 . With the assumption of a parallel-plate capacitor model for dual gates, the slope of the $V_{tg, D} - V_{bg}$ curve is equal to $C_{\text{CCTO}}/C_{\text{SiO}_2}$, the ratio of capacitors between the bottom and top gates. Therefore, we can extract the equivalent oxide thickness (EOT) of the CCTO-550 thin film to be 0.9 nm from this device, confirming the preservation of high k nature in the 2D devices. More CCTO-gated monolayer graphene devices were measured (Supplementary Table 1 and Supplementary Fig. 12), showing the repeatable k of ~ 43 for CCTO with the thickness of 20 nm, which is close to the value from MIM measurements. The consistent results from two measurements confirm its reliable high- k property. Moreover, the EOT can be also deduced from the dual-gate graphene devices (Supplementary Fig. 12). The EOT of 15 nm-thick CCTO films is 1.54 nm which is comparable with those of recently developed high- k dielectrics for 2D devices (Supplementary Table 2).

The level of the leakage current in FETs is also one significant factor when considering new dielectric materials. Therefore, the CCTO-550 films were used as top dielectrics for monolayer graphene (Supplementary Fig. 13), multi-layer MoS₂, and MoSe₂ flakes, respectively. As presented in Fig. 2e, all devices (15 in total) possess an ultralow gate leakage of less than 2×10^{-4} A/cm², two orders of magnitude lower than the low-power (LP) limit (1.5×10^{-2} A/cm²) and far below the metal-oxide-semiconductor FET gate limit (10 A/cm²)³⁷. Moreover, as a new dielectric material for 2D semiconductors, we have investigated its electrical stability by the bias-temperature instabilities (BTI) measurements (Supplementary Fig. 14), showing the comparable recovery behaviors with crystalline h-BN^{7,38}.

CCTO-gated 2D semiconductors FETs

High k and transferrable features stimulate us to mechanically integrate CCTO films with 2D semiconducting materials to form a novel 3D

(amorphous oxide insulator)–2D (channel semiconductors) heterostructure by transfer. We first used the mechanically exfoliated MoS₂ flakes as one exemplification. The standard fabrication process includes the mechanical exfoliation of multilayer MoS₂ flakes, the depositions of source/drain electrodes, the transfer of a CCTO-550 film onto TMD flakes, and the deposition of the top-gate metals (Fig. 3a). The output (drain-source current I_{ds} versus drain-source voltage V_{ds}) and top-gate transfer (I_{ds} versus V_{tg} , measured with the back gate grounded) characteristics are shown in Fig. 3c, respectively. When V_{ds} are small, the linear output curves suggest an ohmic contact between MoS₂ and source/drain electrodes, while with larger V_{ds} , the current saturation occurs. Transfer curves manifested the device as a typical n-type transistor, turning on and off within ± 0.5 V and with an on/off ratio of 10^5 – 10^6 (Supplementary Fig. 15). More strikingly, the best SS of a CCTO-gated MoS₂ transistor is 67 mV/dec at room temperature, which is close to the thermionic limit (60 mV/dec) and among the best records of previously reported MoS₂ FETs (Supplementary Table 3). Moreover, SS is kept small for an extensive range of V_{ds} . According to the equation¹⁸

$$SS = \ln 10 \frac{k_B T}{q} \left(1 + \frac{qD_{it}}{C_{\text{gate}}} \right) \quad (1)$$

where k_B , T , q , D_{it} , and C_{gate} are the Boltzmann constant, absolute temperature, elementary charge, the density of interface trap, and gate capacitance (here, top-gate capacitance) calculated by k and the thickness of the CCTO film, we extracted D_{it} of the CCTO/MoS₂ transistor to be around 1.68×10^{12} cm⁻² eV⁻¹, which was lower than typical values of MoS₂ transistors with ALD high- k top dielectrics (Supplementary Table 3)^{39–41}.

We further applied the double-sweep I_{ds} - V_{tg} measurements and found the ultra-small hysteresis (Fig. 3d). The hysteresis width (ΔV_H) is

normalized by the strength of the electrical field and is listed as functions of the sweep rate and I_{ds} in Fig. 3e. Despite the top-gate voltage range we utilized (-1 V – 1 V , or -2 V – 2 V), ΔV_H negatively correlates with the applied sweep rate and is always less than $10\text{ mV}/(\text{MV cm}^{-1})$ (See the double-sweep transfer curves and detailed analysis ΔV_H versus sweep rate, total sweep time, and frequency in Supplementary Fig. 16). Note that the electrical field strength selected here is 2.66 MV/cm , larger than values when evaluating other high- k dielectrics^{11,18,39}. When fixing the sweep rate to be 0.3 V/s (inset of Fig. 3e), ultrasmall ΔV_H of $-1\text{ mV}/(\text{MV cm}^{-1})$ is found when I_{ds} changes over 4 orders of magnitude, showing the best hysteresis behavior among MoS_2 transistors with the same device configurations^{8,13,40,42,43}. The width of the hysteresis window, in principle, positively correlates with near-interface border traps, which exchange charge with MoS_2 channels on the time scale of measurements⁴⁴. In our experiments, the unprecedentedly small hysteresis in MoS_2 FETs indicates the high quality of high- k oxides and/or semiconductor-insulator interface. The observed nanogap and consequent absence of physical contact between CCTO and TMDs flakes contribute significantly to this low- D_{it} interface. As forementioned, when compared with directly deposited insulators (by like ALD), one concealed advantage of transferred dielectrics shown by previous reports and our experiments here is the existence of the nanogap in between to avoid physical contact to fragile channels and quality degradations. Even when using chemical vapor deposition (CVD)-grown monolayers as channels, the device performance was still very good, boosted by the nanogap^{17,18}. Figure 3f summarizes the hysteresis width and SS obtained in devices of high- k dielectric gated MoS_2 devices, where our results show excellent device performance among high- k dielectrics^{10,13,18,39,40,42,45,46}.

To examine the consistency of device performance induced by CCTO thin films, more MoS_2 devices were investigated, exhibiting consistently good device performance (Supplementary Fig. 17, including small SS and ΔV_H), and good device stability after being stored in air (Supplementary Fig. 18). The CVD-grown monolayer MoS_2 has been utilized as well, followed by its transfer onto SiO_2/Si substrates. By the same integration technique used for exfoliated MoS_2 flakes, CCTO thin films were further incorporated as top dielectrics (Methods). In Supplementary Fig. 19, we show the output characteristics with 0 – 1 V of V_{tg} , top-gate transfer curves under varied V_{ds} (0.1 – 1.5 V), and double-sweep top transfer curve with 1 V of V_{ds} of one CCTO-gated CVD monolayer MoS_2 device, demonstrating the high- k dielectric functionality of CCTO with SS of 95 mV dec^{-1} . Moreover, the norm. hysteresis width of this CCTO/CVD monolayer MoS_2 device is $8\text{ mV}/(\text{MV cm}^{-1})$. Multiple CCTO/ MoSe_2 devices were examined as well (Supplementary Fig. 20), displaying good device performance and leakage current (less than 10^{-4} A cm^{-2}). Furthermore, based on the CVD monolayer MoS_2 , the performance of the device array has been investigated at room temperature and at the practical operation temperature, respectively, demonstrating its large-scale uniformity and thermal stability (Supplementary Note 3 and Supplementary Figs. 21 and 22).

To show the device scaling potential, we fabricated the short-channel device. As shown in Supplementary Fig. 23a, a channel length of $\sim 42\text{ nm}$ is revealed. This short-channel device possesses the on/off ratio of $>10^8$ and a SS of 76 mV/dec . All device performance confirms the good electrostatic control from the top gate with CCTO as high- k dielectrics.

For typical inorganic dielectrics, the band gap is inversely proportional to the dielectric constant^{47,48}. While CCTO itself has a moderate bandgap of $\sim 3.8\text{ eV}$ when compared with some wide bandgap dielectrics (e.g., CaF_2), the leakage currents in CCTO-gated devices exhibit consistently low (See band diagrams in Supplementary Fig. 24). As revealed by STEM imaging (Fig. 1e), the small nanogap ($\sim 1\text{ nm}$) between CCTO and 2D semiconductor channels can contribute significantly to an undamaged semiconductor surface, low density of

interface impurities, and suppressed leakage current. Unlike the bottom-up growth/deposition of oxides on channel materials at evaluated temperatures during the gas-to-solid approaches, where the insulators seamlessly touch and bond with the channel materials, the CCTO film as an intact structure was transferred on top of TMDs flakes at room temperature, producing a physical separation in between, akin to the vdW gap in 2D material heterostructures. Meanwhile, the drawbacks of utilizing high- k materials as gate dielectrics, including the fringing field and remote phonon (polar vibrational modes) scattering^{7,14,18}, could be mitigated to some extent by the physical gap between insulators and channels. From another point of view, very recently there has been a growing trend to explore and utilize the naturally formed nanostructures in 2D semiconductor devices. For instance, when transferring TMDs monolayer on top of pre-fabricated gate, the semiconductor flakes were lifted up to create an air gap (between TMDs and SiO_2 substrates), which plays the critical role in achieving ohmic contacts, low parasitic capacitance, and high-frequency operations⁴⁹. Another instance is the nanogap formed when one MoS_2 flake is partially supported by a h-BN flake, leading to a tunable barrier in a gapped channel for a pseudo complementary metal-oxide-semiconductor architecture⁵⁰. Our results of using nanogap as a device performance booster, together combined with these previously reported findings, demonstrate the high reliability and endurance when leveraging these naturally produced nanostructures in 2D semiconductor devices.

Electrically-manipulated, optically-activated floating gate and in-memory logic operations

Apart from high k , complex oxide CCTO has been demonstrated as a promising, visible-light active photocatalyst to, for example, decompose organic wastes⁵¹. Previous studies showed that the erythrosine (dye) solution turned completely colorless (fully degraded) under visible light in 30 min with the incorporation of CCTO⁵². The photo-generated carriers in CCTO were attributed to the transition from a $\text{Cu}^{2+} + \text{Ti}^{4+}$ ground state to a $\text{Cu}^{3+} + \text{Ti}^{3+}$ excited state^{29,51}. Therefore, in our experiments we further explored the photoresponse and optoelectronic behaviors in CCTO-top-gated MoS_2 devices (Method; Supplementary Fig. 25a). As shown in Fig. 4a, after the illumination of a 0.5 s laser pulse (532 nm , $0.7\text{ nW}/\mu\text{m}^2$; Case *i*), the channel current I_{ds} gets an order of magnitude increase ($\sim 10^{-10}\text{ A}$ under a bias of 1 V) and more importantly, is retained in a non-volatile way. More experiments show that the boosted I_{ds} are stable for at least within $\sim 10^4\text{ s}$ (Fig. 4b). This behavior is in sharp contrast to the TMD flakes' photocurrent, which vanishes to zero in seconds⁵³, highly suggesting that the light-harvesting component responsible for the non-volatile increase of I_{ds} is the CCTO layer in our devices. Moreover, the memory behavior here, that is, storing the light stimulus, is reminiscent of the floating gate transistor in which the electrically isolated gate stores charge⁵⁴. We borrowed the photo-controlled charge transfer process mechanism, previously proposed in silicon-vdW heterostructure, to interpret the memory behavior we obtained here⁵⁵. As shown in Fig. 4c, when the dissociation of photo-generated electron-hole pairs occurs near the bottom surface of CCTO, electrons jump to lower energy levels of TMDs layers by tunneling through the nanogap, leaving holes as an optically-activated floating gate to modulate the channel states by the field effect. Here, by considering the N-type feature of MoS_2 flakes, these charges stored in CCTO (close to the channel) turn on the device and, therefore, are responsible for increased I_{ds} . The nanogap between CCTO and the channel is essential for electrically insulating this floating gate, denying its neutrality by electrons from the channel. We further speculate the active traps in oxides may help visible light harvesting and exciton dissociations, and then serve as the positively charged centers. Note that here, non-volatile optoelectronic memory behaviors are implemented within a single FET configuration, in sharp contrast to 5 layers previously developed to achieve a similar

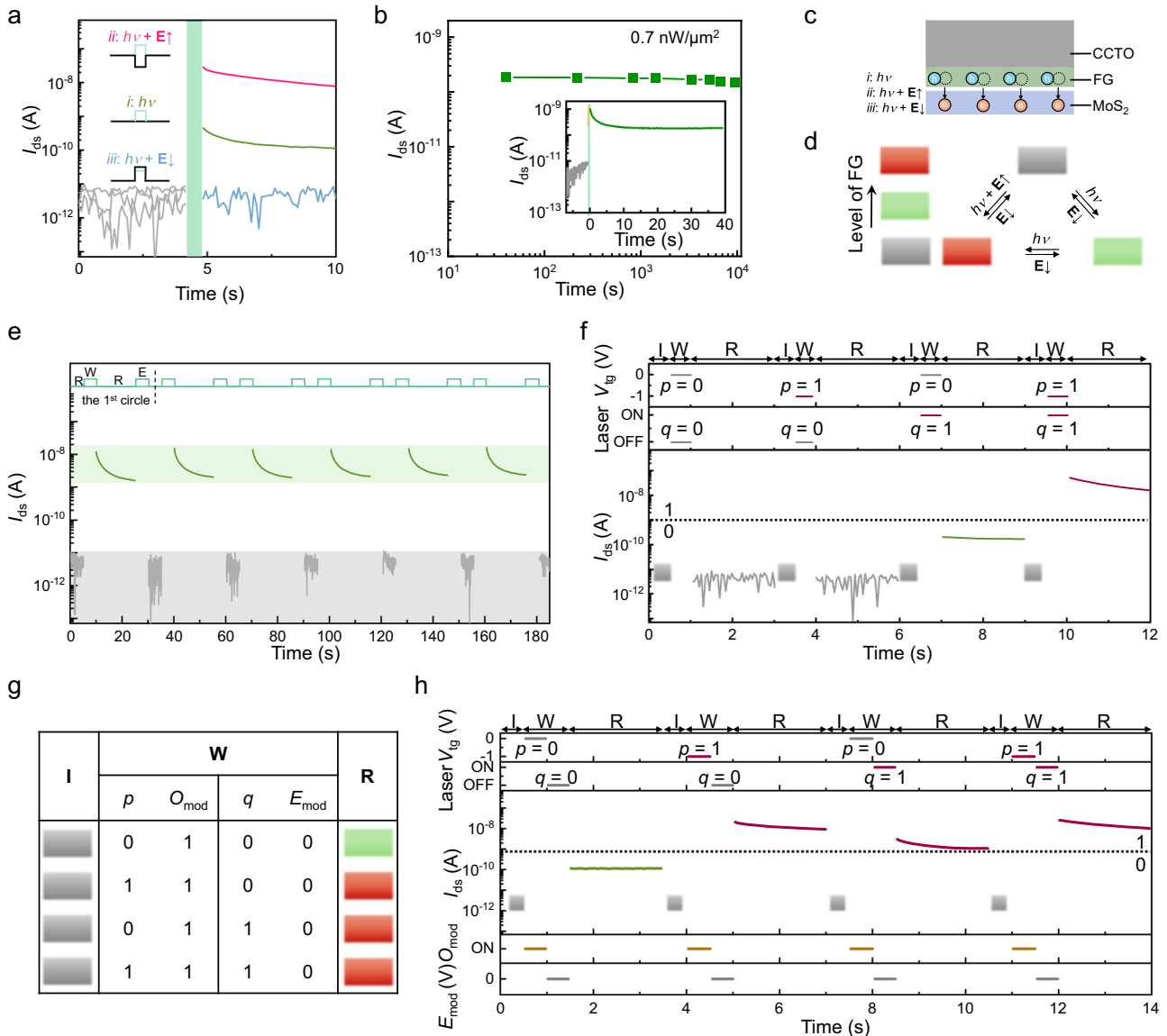


Fig. 4 | Non-volatile optoelectronic memory and logic-in-memory operations. **a** Photoresponse of one CCTO-gated MoS₂ device under pure light stimulus (green, case *i*), the laser illumination with negative V_{lg} (-1 V , red, case *ii*), and light with positive V_{lg} (1 V , blue, case *iii*), respectively. **b** Non-volatile light stimulus memory with high-level I_{ds} (read: $V_{ds} = 1 \text{ V}$) retained for $\sim 10^4 \text{ s}$. Inset: Initial step of photo-response showing an abrupt jump of channel current under the laser illumination and a slight drop after withdrawing laser. **c** Schematic of the optically-activated

floating gate stemming from unnaturalized holes. **d** Schematic of tuning the level of floating gate (FG) by the optical and/or electrical means. **e** Six circles of optical writing and electrical erasing in one device. **f** AND operation with V_{lg} and laser as two independent logic variables and the level of I_{ds} as output. Truth table (**g**) and experimental demonstrate (**h**) of the OR gate with the multiple cycle strategy. The read voltage is 1 V .

function⁵⁶. The reason for this structural simplicity is that the transferred CCTO film serves as a dual-function component, that is, high- k dielectrics sensing and storing the light stimulus.

This optically activated floating gate mechanism is further supported by the electric field-assisted control experiments by applying the laser and V_{lg} simultaneously. As displayed in Fig. 4a, c the amount of tunnelling electron (from CCTO to the channel) and consequently holes stored, in principle, can be enhanced (depressed) by the negative (positive) V_{lg} which leads to the electric field (E) upward (downward), and I_{ds} after withdrawing the optical and electrical stimuli can get increased (decreased) accordingly. And our experiments show precisely the same results. While I_{ds} become three orders of magnitude larger after the combined stimulus of the laser and negative V_{lg} ($E\uparrow$; Case *ii*), in Case *iii* where positive V_{lg} is applied ($E\downarrow$), the channel current maintains the same level as that before the stimuli, or in other

words, no floating gate or memory function takes place. Based on these facts, we conclude that this floating gate is optically activated and can be electrically manipulated (increased/decreased). As shown in Fig. 4c, the level of the floating gate, i.e., the amount of stored charge near the bottom surface of CCTO, can be tuned and switched between different states by means of light and/or electric field, for example, jumping up to a higher level by laser (optically writing) and going down to a lower level by the electric field (electrically erasing). We further show the stability of optically writing and electrically erasing processes. As displayed in Fig. 4e, the CCTO-gated device exhibits repeatable high-level channel current (high-conductance, state “1”) after writing and low-level I_{ds} (low-conductance, state “0”) after erasing, and two different states are well separated and easily distinguished, yielding a switching ratio of ~ 2 orders of magnitude. Moreover, we note that the optically-activated memory behavior is

also light intensity dependent (Supplementary Fig. 26), and under the level of the natural light, CCTO/MoS₂ devices work as the high-performance FETs.

The non-volatile memory behaviors and feasible switching between different stable states by external fields at room temperature allow the implementation of reconfigurable logic-in-memory operations, with $V_{\text{fg}}(p)$ and laser excitation (q) as two inputs and the level of channel current as the electrical read-out output of the logic operation. As displayed in Fig. 4f, after the initiation step (to recover the level of the floating gate back to the lowest state), optical and electrical stimuli are applied simultaneously in the writing (W) step to execute the logic process, followed by a reading (R) step ($V_{\text{ds}} = 1\text{V}$) to readout the channel current and logic value. In this operation, the high-conductance state “1” will be obtained only when both p and q are true, verifying the AND gate. By this single circle process, the nimp operation can be also achieved (Supplementary Fig. 27a, b). Moreover, if adopting the multiple cycle strategy⁵⁷ (Supplementary Note 4) by sequentially applying p and q in different cycles and supplementing the optical (O_{mod}) and electrical modulation (E_{mod}), more logic operations can be implemented. For instance, in Fig. 4g, h, the writing step includes two cycles; p and q are applied in the first and second cycles, respectively, eventually leading to the OR gate. Six more Boolean logic operations (Supplementary Figs. 25c–h and 27c–h) have been achieved by the multiple-cycle approach. In total, nine basic operations can be completed in one CCTO-gated device. Note that in traditional programmable logic circuits, each logic block is function-fixed by factory settings, and a complex routing manner is required⁵⁷. Here, the reconfigurability of logic operations in the single CCTO-gated device demonstrates its potential for high-efficiency in-memory computing in 2D materials devices^{2,5}.

Discussion

The Pechini method, characterized as a liquid-to-solid solution process, provides significant versatility in preparing thin films of various complex oxides. This technique is notably cost-effective and efficient, primarily due to its use of a wet-chemistry process, bypassing the need for large-scale vacuum equipment typically associated with thin film fabrication. The lateral dimensions of these films can be adapted, constrained only by the size of the substrates employed. Also, different metal salts can be used as precursors. As the examples, thin films of columbite-type amorphous zirconium titanate (α -ZrTiO) and hafnium titanate (α -HfTiO) are prepared successfully by the Pechini method (Supplementary Note 5, Supplementary Fig. 28). After the transfer, these resulting films preserved high- k dielectric properties as well, demonstrating the generality of this method. Apart from its generality, the combination of the high- k dielectric property and the capability of sensing light and storing charge renders CCTO unique and sets it apart from transferrable oxide layers previously reported^{11,13,16,17,43,58}. Moreover, isolating the oxide layer to be a free-standing film by etching the conventional substrate with proper alkaline solution may also be applicable to other oxides, for example, an alloy of perovskite oxides BaHf_{0.6}Ti_{0.4}O₃ with an ultrahigh k (~150), offering more dielectric candidates for 2D devices⁵⁹. Last but not least, the wafer-scale fabrication of uniform CCTO thin films by the conventional vacuum deposition (e.g., sputtering)⁶⁰, followed by the etching-transfer process, could be worthy of further investigation.

We have reported the preparation of amorphous perovskite CCTO by the solution-processed Pechini method and its applications as high- k , multifunctional dielectrics in 2D materials electronic devices, presenting a prototype device of photoactive, reconfigurable in-sensor computing-based on 2D semiconductors. The single-metal ion-level chelation ensured the spatial homogeneity of complex oxides. Moreover, the transferrable feature and the preservation of dielectric properties after transfer made it compatible with 2D materials to form heterostructures. Such CCTO-gated MoS₂ devices exhibited SS down

to 67 mV dec⁻¹ and hysteresis width as small as -1 mV/(MV cm⁻¹), confirming the high qualities at interfaces. Furthermore, we have demonstrated that the Pechini-derived CCTO films worked for CVD-grown TMDs. The visible-light-sensitive nature of CCTO, combined with the nanogap architecture in transferred heterostructures, led to an electrically manipulated, optically-activated floating gate in CCTO to sense and store the light stimulus in a non-volatile means. Nine basic logic-in-memory Boolean operations are implemented accordingly in a simple FET architecture. This Pechini-based method can be applicable to other conventional, perovskite complex oxides with high dielectric properties and transferable features, enriching the library of emergent 2D amorphous materials^{61–64}. Our results, as the first occurrence of the solution-derived and dual-function dielectrics in 2D devices, pave the way for in-memory computing in 3D oxides/2D materials heterostructures.

Methods

Preparation of CCTO films

Calcium nitrate tetrahydrate (Ca(NO₃)₂·4H₂O, 99%), copper(II) nitrate trihydrate (Cu(NO₃)₂·3H₂O, 99.99%), tetrabutyl titanate (C₁₆H₃₆O₄Ti, 99%), citric acid monohydrate (C₆H₈O₇·H₂O, 99.5%), and ethylene glycol ((CH₂OH)₂, AR) were utilized as precursors. A stoichiometric amount of Ca(NO₃)₂·4H₂O and Cu(NO₃)₂·3H₂O were first dissolved into ethanol, followed by adding C₆H₈O₇·H₂O and stirring for 1 h to obtain Solution I. Separately, a stoichiometric amount of C₁₆H₃₆O₄Ti was dissolved into ethanol and stirred for 1 h; after adding C₆H₈O₇·H₂O, keep stirring for another hour to obtain Solution II. Then Solutions I and II were mixed, followed by adding ethylene glycol and stirring for 1 h to obtain a homogeneous, blue solution. By the spin coating process (at 4000 rpm for 60 s), the solution layer was deposited on various substrates, including the commercial SiO₂/Si substrate in most cases and quartz for spectroscopic characterizations. Substrates with coated thin films were loaded into a Muffle furnace, in which the films were heated to set temperatures at a rate of 5 min/°C and maintained for 2 h.

Preparation of ZTO films

Zirconium (IV) nitrate pentahydrate (Zr(NO₃)₄·5H₂O, 99.9%), tetrabutyl titanate (C₁₆H₃₆O₄Ti, 99%), citric acid monohydrate (C₆H₈O₇·H₂O, 99.5%), and ethylene glycol ((CH₂OH)₂, AR) were utilized as precursors. After a similar solution process to that of CCTO, a homogeneous, yellow solution was obtained. The deposition and calcination processes were similar to those of CCTO films.

Preparation of HTO films

Hafnium (IV) Dichloride Oxide Octahydrate (HfOCl₂·8H₂O, AR), tetrabutyl titanate (C₁₆H₃₆O₄Ti, 99%), citric acid monohydrate (C₆H₈O₇·H₂O, 99.5%), and ethylene glycol ((CH₂OH)₂, AR) were utilized as precursors. A homogeneous, colorless, and transparent solution was prepared by a similar dissolution process with CCTO. The deposition and calcination processes were similar to those of CCTO films.

Transfer of amorphous oxide thin films

By taking CCTO films as an example, the polymethyl methacrylate (PMMA) solution (495 K, A4, MicroChem) was spin-coated onto calcinated CCTO films, followed by a baking process at 180 °C for 1 min. The whole chip was immersed in an aqueous KOH solution (1 M) to etch the underlying SiO₂/Si substrate. After ~3 h, one PMMA-protected CCTO film was separated from the substrate, forming a self-supporting and floating film. This film was washed several times in deionized water and then loaded onto a target substrate. Naturally drying was conducted for >30 min to completely drain any residual interfacial water. The PMMA film was then removed by a hot acetone bath. The transfer of other types of amorphous oxide thin films possesses the same process.

Note that by this transfer method, CCTO films obtained at high temperatures (≥ 600 °C) cannot be peeled off, probably due to the strong adhesion of CCTO to the Si/SiO₂ substrate when calcining at high temperatures.

Growth and transfer of CVD monolayer MoS₂

The CVD MoS₂ film was prepared by the active chalcogen monomer supply method. The sapphire substrate was treated with O₂ plasma first for cleaning. Then the silica fiber fabric was immersed in Na₂MoO₄ aqueous solution with a concentration of 12 mg/mL. Subsequently, the silica fiber fabric and the sapphire substrate were spaced by mica and placed on a ZnS plate. The system was loaded in one hot-wall tube furnace and ramped to 780 °C, followed by one growth run, which was carried out for 60 min at the low-pressure condition (~ 120 Pa). After the growth, the system was naturally cooled down to room temperature. The as-growth MoS₂ film was transferred onto Si/SiO₂ substrate using the polymethylmethacrylate (PMMA) based technique.

Characterizations

AFM measurements (Dimension Icon, Bruker Corporation) were performed to investigate the surface roughness and thickness of films. XRD data were acquired by a Smart Lab 9KW with Cu K α radiation. X-ray photoelectron spectroscopy (XPS) spectra were obtained with an AXIS Supra apparatus (Kratos Analytical Ltd). The SmartRaman confocal-micro-Raman module was utilized for the Raman measurements with a 100 \times (NA = 0.9) objective lens, coupled with a Horiba iHR320 spectrometer and a charge-coupled device (CCD) detector. UV-Vis-NIR transmittance spectra measurements were conducted by Agilent Cary 7000 spectrophotometer. For cross-sectional STEM characterizations, a dual-beam FIB system (Thermo Scientific Scios 2) was employed to prepare cross-sectional samples for STEM characterizations. Initially, a 200 nm protective layer composed of carbon (C) was deposited using FIB e-beam deposition. Subsequently, to safeguard the region of interest during milling, a 1 μ m thick Pt strap layer was deposited after tilting the sample at an angle of 52° relative to the ion beam. A gallium ion (Ga⁺) beam operating at 30 kV with a current ranging from 0.1 to 1 nA was applied to reduce the specimen's thickness to about 50 nm for subsequent STEM investigations. STEM experiments were performed in a JEOL JEM-ARM300F operated at 300 kV with a 23 pA beam. For STEM imaging, the electron beam was converged to 0.14 nm with a convergence semi-angle ~ 22 mrad with 30 μ m condenser lens aperture to scan the sample. The collection semi-angle was 54–220 mrad. All data were collected and analyzed using Digital Micrograph. The band offset characteristic was probed through a UPS (Nexsa, Thermo Fisher).

Device fabrication and measurements

For C-V characterizations, the CCTO films were transferred on Au (100 nm)/SiO₂/Si substrates. Top electrodes with different radii were patterned by standard electron-beam lithography (EBL, ZEPTOOLS ZEL304G), followed by the metal deposition (70 nm of Au) and conventional lift-off process. Regarding the dual-gated FETs, graphene and MoS₂ were mechanically exfoliated on SiO₂/Si substrates by the thermally-assisted transfer technique and identified by the optical microscope first. As for the CVD-MoS₂ FETs, the transferred CVD-MoS₂ was first patterned by standard EBL process and SF₆/O₂ plasma etching. Source and drain electrodes were fabricated by standard EBL and metal depositions. Then, CCTO films were transferred onto the patterned MoS₂ chips. For devices used in electrical and optoelectronic measurements, the top electrodes were prepared using a standard EBL program, and transferred graphene was used as the top electrode, respectively. In/Au (10 nm/40 nm) was used as source/drain electrodes and 70 nm of Au was used as the top-gate electrode. Before the electric measurements, the dual-gated FETs and CVD-MoS₂ FETs were thermally annealed at 190 °C under 500 sccm of Ar for 1 h. The C-V

measurements were carried out in a probe station with a Keysight B1500A semiconductor parameter analyzer. Electrical measurements of dual-gated FETs and CVD-MoS₂ FETs were carried out in a vacuum probe station ($\sim 3 \times 10^{-6}$ Torr, ZEPTOOLS, LNP50-4) at room temperature by a Keithley 2614B and 2401 SourceMeter. A green single longitudinal mode laser (CNI laser, MSL-FN-532) whose wavelength is 532 nm was used for optoelectronic measurements. The power density of the light at the position of the samples was measured by a PM-100D power meter (Thorlabs). The spot diameter of the incident light was around 30 μ m, which ensures full coverage of the device positioned at the center of the light spot. The ON/OFF switching time of the light was controlled by a SC10 optical beam shutter (Thorlabs).

Data availability

The data supporting the findings of this study are included in the paper and its Supplementary Information. All data are available from the corresponding author on request. Source data are provided with this paper⁶⁵.

References

1. Wang, S., Liu, X. & Zhou, P. The road for 2D semiconductors in the silicon age. *Adv. Mater.* **34**, 2106886 (2022).
2. Yin, L., Cheng, R., Wen, Y., Liu, C. & He, J. Emerging 2D memory devices for in-memory computing. *Adv. Mater.* **33**, 2007081 (2021).
3. Akinwande, D. et al. Graphene and two-dimensional materials for silicon technology. *Nature* **573**, 507–518 (2019).
4. Geim, A. K. & Grigorieva, I. V. Van der Waals heterostructures. *Nature* **499**, 419–425 (2013).
5. Migliato Marega, G. et al. Logic-in-memory based on an atomically thin semiconductor. *Nature* **587**, 72–77 (2020).
6. Mennel, L. et al. Ultrafast machine vision with 2D material neural network image sensors. *Nature* **579**, 62–66 (2020).
7. Illarionov, Y. Y. et al. Insulators for 2D nanoelectronics: the gap to bridge. *Nat. Commun.* **11**, 3385 (2020).
8. Li, W. et al. Uniform and ultrathin high-*k* gate dielectrics for two-dimensional electronic devices. *Nat. Electron.* **2**, 563–571 (2019).
9. Xu, Y. et al. Scalable integration of hybrid high-*k* dielectric materials on two-dimensional semiconductors. *Nat. Mater.* **22**, 1078–1084 (2023).
10. Illarionov, Y. Y. et al. Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. *Nat. Electron.* **2**, 230–235 (2019).
11. Lu, Z. et al. Wafer-scale high-*k* dielectrics for two-dimensional circuits via van der Waals integration. *Nat. Commun.* **14**, 2340 (2023).
12. Lu, D. et al. Monolithic three-dimensional tier-by-tier integration via van der Waals lamination. *Nature* **630**, 340–345 (2024).
13. Zeng, D. et al. Single-crystalline metal-oxide dielectrics for top-gate 2D transistors. *Nature* **632**, 788–794 (2024).
14. Luo, P. et al. Molybdenum disulfide transistors with enlarged van der Waals gaps at their dielectric interface via oxygen accumulation. *Nat. Electron.* **5**, 849–858 (2022).
15. Xu, W. et al. Single-crystalline high-*k* GdOCl dielectric for two-dimensional field-effect transistors. *Nat. Commun.* **15**, 9469 (2024).
16. Yi, K. et al. Integration of high-*k* native oxides of gallium for two-dimensional transistors. *Nat. Electron.* **7**, 1126–1136 (2024).
17. Yang, A. J. et al. Van der Waals integration of high-*k* perovskite oxides and two-dimensional semiconductors. *Nat. Electron.* **5**, 1–8 (2022).
18. Huang, J.-K. et al. High-*k* perovskite membranes as insulators for two-dimensional transistors. *Nature* **605**, 262–267 (2022).
19. Li, S., Liu, X., Yang, H., Zhu, H. & Fang, X. Two-dimensional perovskite oxide as a photoactive high-*k* gate dielectric. *Nat. Electron.* **7**, 216–224 (2024).
20. Liu, C. et al. Two-dimensional materials for next-generation computing technologies. *Nat. Nanotechnol.* **15**, 545–557 (2020).
21. Yang, A. J. et al. Multifunctional magnetic oxide-MoS₂ heterostructures on silicon. *Adv. Mater.* **35**, 2302620 (2023).

22. Kim, Y.-H. et al. Flexible metal-oxide devices made by room-temperature photochemical activation of sol-gel films. *Nature* **489**, 128–132 (2012).
23. Park, J. W., Kang, B. H. & Kim, H. J. A review of low-temperature solution-processed metal oxide thin-film transistors for flexible electronics. *Adv. Funct. Mater.* **30**, 1904632 (2020).
24. Liu, J., Smith, R. W. & Mei, W.-N. Synthesis of the giant dielectric constant material $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ by wet-chemistry methods. *Chem. Mater.* **19**, 6020–6024 (2007).
25. Subramanian, M. A., Li, D., Duan, N., Reisner, B. A. & Sleight, A. W. High dielectric constant in $\text{ACu}_3\text{Ti}_4\text{O}_{12}$ and $\text{ACu}_3\text{Ti}_3\text{FeO}_{12}$ phases. *J. Solid State Chem.* **151**, 323–325 (2000).
26. Lin, J., Yu, M., Lin, C. & Liu, X. Multiform oxide optical materials via the versatile pechini-type sol-gel process: synthesis and characteristics. *J. Phys. Chem. C* **111**, 5835–5845 (2007).
27. Nakanishi, K. Macroporous morphology control by phase separation. In *Proc. Handbook of Sol-Gel Science and Technology* (eds. Klein, L., Aparicio, M. & Jitianu, A.) 1–32 (Springer International Publishing, Cham, 2016).
28. Sunde, T. O. L., Grande, T. & Einarsrud, M.-A. Modified pechini synthesis of oxide powders and thin films. In *Proc. Handbook of Sol-Gel Science and Technology* (eds. Klein, L., Aparicio, M. & Jitianu, A.) 1–30 (Springer International Publishing, Cham, 2016).
29. Kawrani, S., Boulou, M., Cornu, D. & Bechelany, M. From synthesis to applications: copper calcium titanate (CCTO) and its magnetic and photocatalytic properties. *ChemistryOpen* **8**, 922–950 (2019).
30. Liu, L. et al. Controlled oxidative functionalization of monolayer graphene by water-vapor plasma etching. *Carbon* **50**, 3039–3044 (2012).
31. Zallen, R. *The Physics of Amorphous Solids*. (John Wiley & Sons, 2008).
32. Li, H. et al. From bulk to monolayer MoS_2 : evolution of Raman scattering. *Adv. Funct. Mater.* **22**, 1385–1390 (2012).
33. Li, R. et al. Valley polarization in superacid-treated monolayer MoS_2 . *ACS Appl. Electron. Mater.* **2**, 1981–1988 (2020).
34. Liu, C. et al. Controllable van der Waals gaps by water adsorption. *Nat. Nanotechnol.* **19**, 448–454 (2024).
35. Mao, P. et al. Grain size effect on the dielectric and non-ohmic properties of $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ ceramics prepared by the sol-gel process. *J. Alloys Compd.* **778**, 625–632 (2019).
36. Yuan, Y. et al. A distributed bulk-oxide trap model for Al_2O_3 InGaAs MOS devices. *IEEE Trans. Electron Devices* **59**, 2100–2106 (2012).
37. Robertson, J. High dielectric constant oxides. *Eur. Phys. J. Appl. Phys.* **28**, 265–291 (2004).
38. Illarionov, Y. Y. et al. The role of charge trapping in $\text{MoS}_2/\text{SiO}_2$ and MoS_2/hBN field-effect transistors. *2D Mater.* **3**, 035004 (2016).
39. Wen, M., Xu, J., Liu, L., Lai, P.-T. & Tang, W.-M. Effects of annealing on electrical performance of multilayer MoS_2 transistors with atomic layer deposited HfO_2 gate dielectric. *Appl. Phys. Express* **9**, 095202 (2016).
40. Liu, H. & Ye, P. D. MoS_2 dual-gate MOSFET with atomic-layer-deposited Al_2O_3 as top-gate dielectric. *IEEE Electron Device Lett.* **33**, 546–548 (2012).
41. Zou, X. et al. Interface engineering for high-performance top-gated MoS_2 field-effect transistors. *Adv. Mater.* **26**, 6255–6261 (2014).
42. Uchiyama, H., Maruyama, K., Chen, E., Nishimura, T. & Nagashio, K. A monolayer MoS_2 FET with an EOT of 1.1 nm achieved by the direct formation of a high- k Er_2O_3 insulator through thermal evaporation. *Small* **19**, 2207394 (2023).
43. Zhu, C. Y. et al. Magnesium niobate as a high- k gate dielectric for two-dimensional electronics. *Nat. Electron.* **7**, 1137–1146 (2024).
44. Illarionov, Y. Y. et al. Energetic mapping of oxide traps in MoS_2 field-effect transistors. *2D Mater.* **4**, 025108 (2017).
45. Liu, K. et al. A wafer-scale van der Waals dielectric made from an inorganic molecular crystal film. *Nat. Electron.* **4**, 906–913 (2021).
46. Li, T., Wan, B., Du, G., Zhang, B. & Zeng, Z. Electrical performance of multilayer MoS_2 transistors on high- k Al_2O_3 coated Si substrates. *AIP Adv.* **5**, 057102 (2015).
47. Robertson, J. Band offsets of wide-band-gap oxides and implications for future electronic devices. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.* **18**, 1785–1791 (2000).
48. Wang, B. et al. High- k gate dielectrics for emerging flexible and stretchable electronics. *Chem. Rev.* **118**, 5690–5754 (2018).
49. Fan, D. et al. Two-dimensional semiconductor integrated circuits operating at gigahertz frequencies. *Nat. Electron.* **6**, 879–887 (2023).
50. Wei, X. et al. Homojunction-loaded inverters based on self-biased molybdenum disulfide transistors for sub-picowatt computing. *Nat. Electron.* **7**, 138–146 (2024).
51. Clark, J. H. et al. Visible light photo-oxidation of model pollutants using $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$: an experimental and theoretical study of optical properties, electronic structure, and selectivity. *J. Am. Chem. Soc.* **133**, 1016–1032 (2011).
52. Kushwaha, H. S. et al. Efficient solar energy conversion using $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ photoanode for photocatalysis and photoelectrocatalysis. *Sci. Rep.* **6**, 18557 (2016).
53. Zhang, S. et al. Laser annealing towards high-performance monolayer MoS_2 and WSe_2 field effect transistors. *Nanotechnology* **31**, 30LT02 (2020).
54. Kahng, D. & Sze, S. M. A floating gate and its application to memory devices. *Bell Syst. Tech. J.* **46**, 1288–1295 (1967).
55. Lee, M.-P. et al. Silicon–van der Waals heterointegration for CMOS-compatible logic-in-memory design. *Sci. Adv.* **9**, eadk1597 (2023).
56. Zhu, R. et al. Non-volatile optoelectronic memory based on a photosensitive dielectric. *Nat. Commun.* **14**, 5396 (2023).
57. Li, J. et al. Room-temperature logic-in-memory operations in single-metallofullerene devices. *Nat. Mater.* **21**, 917–923 (2022).
58. Yin, L. et al. High- k monocrystalline dielectrics for low-power two-dimensional electronics. *Nat. Mater.* <https://doi.org/10.1038/s41563-024-02043-3> (2024).
59. Song, D. et al. High- k perovskite gate oxide for modulation beyond 10^{14} cm^{-2} . *Sci. Adv.* **8**, eabm3962 (2022).
60. Han, C. S., Choi, H. R., Choi, H. J. & Cho, Y. S. Origin of abnormal dielectric behavior and chemical states in amorphous $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ thin films on a flexible polymer substrate. *Chem. Mater.* **29**, 5915–5921 (2017).
61. Tian, H. et al. Disorder-tuned conductivity in amorphous monolayer carbon. *Nature* **615**, 56–61 (2023).
62. Tian, H., Yao, Z., Li, Z., Guo, J. & Liu, L. Unlocking more potentials in two-dimensional space: disorder engineering in two-dimensional amorphous carbon. *ACS Nano* **17**, 24468–24478 (2023).
63. Liu, S. et al. Degree of disorder-regulated ion transport through amorphous monolayer carbon. *RSC Adv* **14**, 17032–17040 (2024).
64. Liu, L. When 2D Materials encounter disorder. *Chin. Phys. Lett.* **40**, 056101 (2023).
65. Yao, Z. Transferrable, wet-chemistry-derived high- k amorphous metal oxide dielectrics for two-dimensional electronic devices (TWcdHAMODfDED). *figshare* <https://doi.org/10.6084/m9.figshare.28159805> (2025).

Acknowledgements

This work was supported by the Beijing Natural Science Foundation (JQ23004 to L.L.), National Key R&D Program of China (2021YFA1400500 to L.L., 2024YFA1207701 to L.W.), National Natural Science Foundation of China (12474161 to L.L., 52403368 to H.T., 52322311 to L.W., 52461160301 to L.W., W2442018 to S.U.), and China Postdoctoral Science Foundation (BX20230002 to H.T., 2024M760069 to H.T.). This work was partially supported by the Creative Materials Discovery Program of the Ministry of Science and ICT (2018M3D1A1058536 to Y.S.C.), Republic of Korea. L.W. is grateful for

the support from the Youth Innovation Promotion Association of CAS (2020009 to L.W.). L.L. acknowledges the supports of facilities from Peking Nanofab. We thank Materials Processing and Analysis Center, Peking University for assistance with XRD, XPS, SEM, TEM, and EDS characterizations.

Author contributions

J.G. and L.L. conceived the project. Z.Y. and H.T. contributed equally. Z.Y., S.U., Z.L., P. Liao, Y.S.J., and Y.S.C. carried out the CCTO preparations and transfer. J.H., G.X., K.L., Y.Z., and Z.Y. performed the CVD growth of TMDs monolayer. Z.Y., H.T., and R.L. performed the exfoliation of TMDs. Z.Y., G.Y., H.T., P.Liao, Y.L., W.L., Y.W., and L.Y.Z. performed the general characterizations (AFM, Raman, XRD, UV-Vis-NIR transmittance spectra, etc.). H.S., L.W., and P. Liu carried out the TEM samples' preparation (FIB) and characterizations. Z.Y., H.T., R.L., and X.Z. performed the device fabrications. Z.Y. and H.T. performed the device measurements and data analysis. L.W., Y.S.C., and J.G. provided insightful remarks and suggestions. J.G. and L.L. wrote the manuscript with contributions from Z.Y. and H.T. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at <https://doi.org/10.1038/s41467-025-56815-9>.

Correspondence and requests for materials should be addressed to Junjie Guo or Lei Liu.

Peer review information *Nature Communications* thanks Cheng-Yan Xu and the other, anonymous, reviewer(s) for their contribution to the peer review of this work. A peer review file is available.

Reprints and permissions information is available at <http://www.nature.com/reprints>

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License, which permits any non-commercial use, sharing, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if you modified the licensed material. You do not have permission under this licence to share adapted material derived from this article or parts of it. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by-nc-nd/4.0/>.

© The Author(s) 2025